Datasheet

FS9932

8-Bit MCU with 2k program ROM, 128-byte data RAM,
1 low noise OPAMP, 6-ch 14-Bit ADC,
4 × 12 LCD driver and RTC.

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Contents

1. General Description

The FS9932 is a high performance, low cost CMOS 8-bit single chip microcontroller with an embedded 2kx16 bit ROM, a 6-channel 14-bit fully differential input analog to digital converter, a low noise amplifier, and a 4 x 12 LCD driver.

The FS9932 is best suited for applications such as low cost body scale, barometer, hygrometer, etc.

2. Features

- 8-bit microcontroller, 37 single word instructions.
- Embedded 2k x 16 bit program memory, 128-byte data memory.
- CPU operation voltage range is from 2.4V to 3.6V.
- Embedded 1.25 MHz oscillator.
- External 32768Hz crystal oscillator (RTC) or 4MHz crystal oscillator (Mask options are FS9932L for 32768Hz and FS9932H for 4MHz).
- Operation current is about 1.5mA; sleep mode current is about 2μA.
- 6-layer hardware stacks.
- 3 Interrupt sources (external: Input Port, internal: Timer, ADC).
- 6 analog input channels
- 14-bit noise free ADC with programmable output rate and resolution.
- Embedded charge pump circuit (Voltage Doubler) and voltage regulator (3.4V regulated output).
- Embedded bandgap voltage reference (typical 1.2V±50mV, 100ppm/°C).
- Internal silicon temperature sensor.
- Low noise (1μV peak-to-peak without chopper, 0.5μV peak-to-peak with chopper, 0.1Hz~1Hz) OPAMP with chopper controller.
- 10-bit bi-directional I/O port including 1-bit for buzzer output and 1-bit for PDM output.
- 4 x 12 LCD driver (3V peak-to-peak) and 4-bit programmable output port.
- Watchdog timer.
- Package: dice form (52 pins), 64-pin LQFP.

3. Applications

- Simple electronic scales: body scale, kitchen scale, pocket scale, etc.
- Barometer
- Hygrometer
- Body fat meter
- Thermometer
- Other sensor or transducer measurement application

4. Ordering Information

Product Number	Description	Package Type
FS9932-Mnnn	FS9932 is 14-bit ADC version. (ADO [15:0] is all effective)	Die form (52 pads)
FS9934-Hnnn	FS9934 is 11-bit ADC version. (ADO [2:0] is always “0”)	Die form (52 pads)
FS9934B-Hnnn	FS9934B is 12-bit ADC version. (ADO [1:0] is always “0”)	Die form (52 pads)
FS9932-Mnnn-PCE	FS9932 is 14-bit ADC version. (ADO [15:0] is all effective)	64-pin LQFP (Pb free package)
FS9934-Hnnn-PCE	FS9934 is 11-bit ADC version. (ADO [2:0] is always “0”)	64-pin LQFP (Pb free package)
FS9934B-Hnnn-PCE	FS9934B is 12-bit ADC version. (ADO [1:0] is always “0”)	64-pin LQFP (Pb free package)

Note 1: Code number (MnnnV) is assigned for customer.

Note 2: Mask option (M = L for 32768Hz or H for 4MHz crystal); Code number (nnn = 001~999).

Note 3: For FS9934 shuttle bus, please use below instruction to simulate to read out the real FS9934 ADO.

```
        MOVFW   ADOL
        ANDLW   0F8h
        MOVWF   AL
        MOVFW   ADOH
        MOVWF   AH

;       Now the AH:AL is the ADO, and AL [2:0] is “0”.
;       Normally, we will use AH:AL divided by 1000b to a new ADO1 for the real usage in program.
```

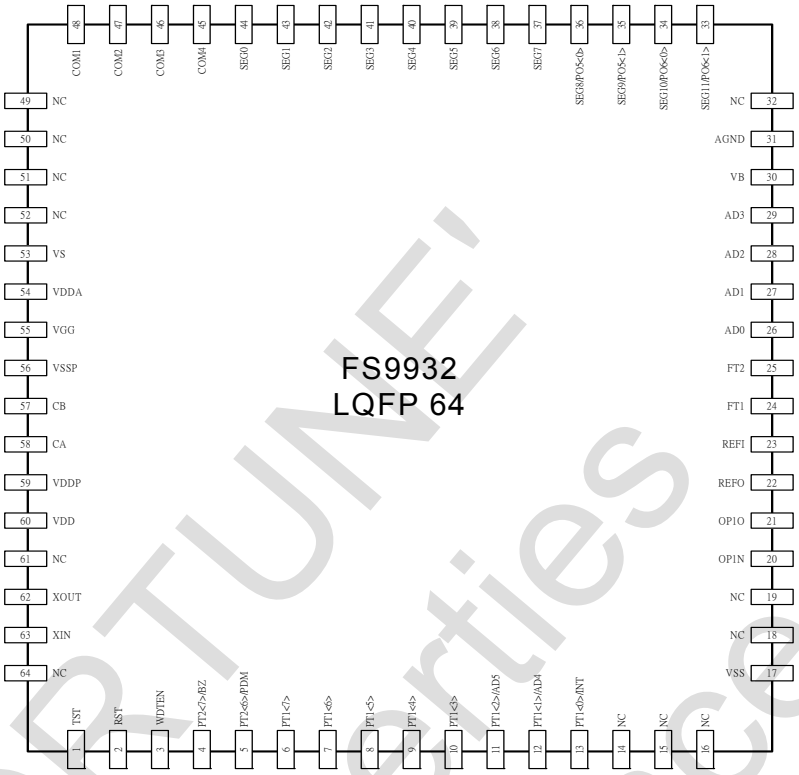
Note 4: For FS9934B shuttle bus, please use below instruction to simulate to read out the real FS9934B ADO.

```
        MOVFW   ADOL
        ANDLW   0FCh
        MOVWF   AL
        MOVFW   ADOH
        MOVWF   AH

;       Now the AH:AL is the ADO, and AL [1:0] is “0”.
;       Normally, we will use AH:AL divided by 100b to a new ADO1 for the real usage in program.
```

1. when the HOLD key is pressed longer than 2 seconds; then, press the key again longer than 2 seconds, the backlight control signal will be shut off. If the HOLD Key is not pressed longer than 2 seconds after the backlight source is started, the light source will be shut off automatically in 10 seconds.

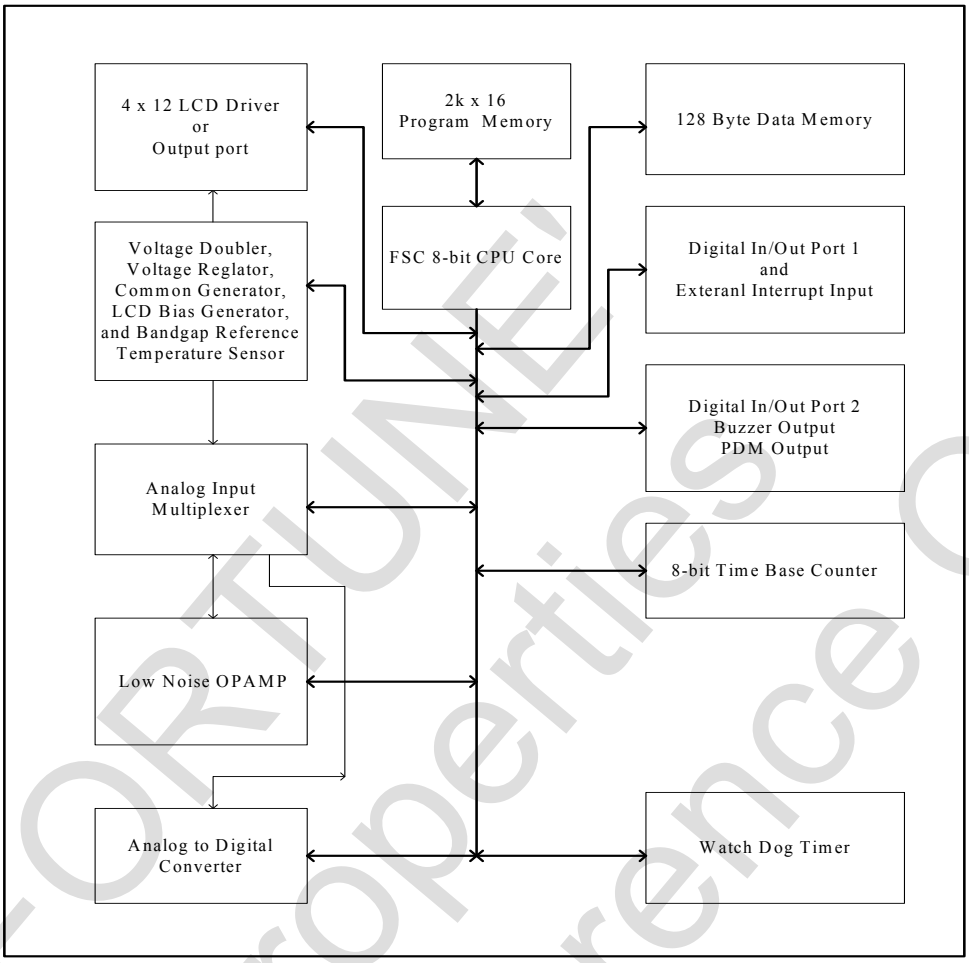
5. Pin Configuration



6. Pin Description

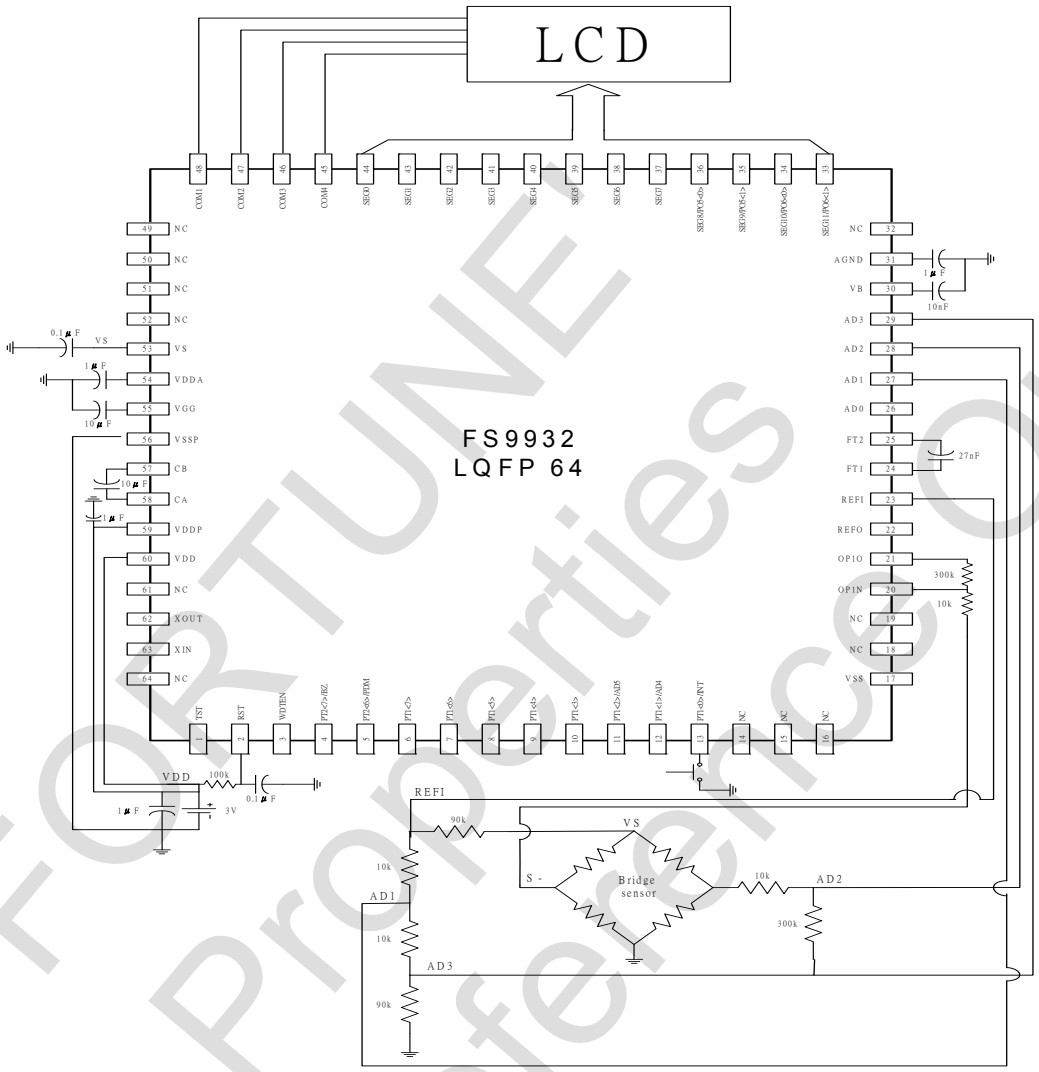
Name	In/Out	Pin No	Description
TST	I	1	Testing Mode
RST	I	2	CPU Reset
WDTEN	I	3	Watchdog Timer Enable Control
PT2<7>/BZ	I/O	4	I/O Port 2 or Buzzer output
PT2<6>/PDM	I/O	5	I/O Port 2 or PDM output
P1<7>~P1<0>	I/O	6~13	I/O Port 1
VSS	I	17	Negative Power Supply (Ground)
OP1N	I	20	OPAMP 1 Negative Input
OP1O	I	21	OPAMP 1 Output
REFO	O	22	Band gap Reference Output
REFI	I	23	ADC Reference Voltage Input
FT1, FT2	I/O	24,25	ADC Pre-Filter Capacitor Connection
AD0~AD3	I	26~29	Analog Input Channel
VB	I	30	Analog Circuit Bias Current Input
AGND	I/O	31	Analog Ground
SEG11~SEG8	O	33~36	LCD Segment Driver Output / Output port
SEG7~SEG0	O	37~44	LCD Segment Driver Output
COM4~COM1	O	45~48	LCD Common Driver Output
VS	O	53	Voltage Source
VDDA	O	54	Analog Power Output
VSSP	I	56	Charge Pump Negative Power Supply
VGG	O	55	Charge Pump Voltage
CB	I/O	57	Charge Pump Capacitor Negative Connection
CA	I/O	58	Charge Pump Capacitor Positive Connection
VDDP	I	59	Charge Pump Positive Power Supply
VDD	I	60	Positive Power Supply
XOUT	O	62	32768Hz or 4MHz Oscillator Output (Mask option)
XIN	I	63	32768Hz or 4MHz Oscillator Input (Mask option)
NC			No Connection

7. Functional Block Diagram



8. Typical Application Circuit

8.1 Scale (Load Cell) Application Circuit



9. Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage to Ground Potential	-0.3 to 5.0	V
Applied Input/Output Voltage	-0.3 to VDD+0.3	V
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

10. Electrical Characteristics

10.1 DC Characteristics (VDD=3V, T_A=25℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDD	Recommend Operation Power Voltage		2.4		3.6	V
IDD1	Supply Current1	Internal Oscillator CPU Operation Power Block all On, ADC, OPAMP On		1.5		mA
IDD2	Supply Current2	Ext 32768Hz CPU Operation		6		μA
IPO	Sleep Mode Supply Current	Sleep, LVR enable		2		μA
VIH	Digital Input High Voltage	PT1, Reset	0.7xVDD			V
		PT2	0.6xVDD			V
VIL	Digital Input Low Voltage	PT1, Reset			0.3xVDD	V
		PT2			0.4xVDD	V
Ipu	Pull up Current	Vin=0		5	10	μA
IOH	High Level Output Current	VOH=0.9xVDD		1		mA
IOL	High Level Output Current	VOL=0.1xVDD		2		mA
VDDA	Analog Power			3.4		V
KVCVDDA	Analog Power Supply Voltage Coefficient		-2		2	%/V
VSR	Voltage Source Switch Resistor			10		Ω
VREF	Build in Reference Voltage	To AGND		1.20		V
KTCREF	VREF Temperature Coefficient	T_A=0~50℃		100		ppm/℃
VLBAT	Low Battery Detector Voltage	S_LB [2:0]=011		2.4		V
VLCD	LCD Driver Peak to Peak Voltage		2.6	2.8	3.0	V
FCK2	Internal RC oscillator			1.25		MHz

10.2 ADC Characteristics (VDD=3V, T_A=25℃, unless otherwise noted)

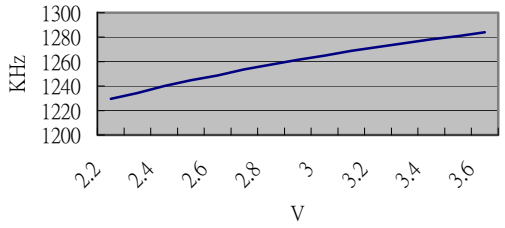
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VAIN	ADC Differential Input Range	To VSS	1		2.2	V
VRFIN	ADC Reference Input Range	(VRH, VRL), ADC Gain=1	0.25		0.5	V
	Resolution	14-bit ADC version		±15625		Counts
	ADC Linearity Error	VRFIN=0.44V 14-bit ADC version	-0.1	0	+0.1	mV
	Resolution	11-bit ADC version, ADO [15:0] divided by 1000b		±1953		Counts
	ADC Linearity Error	VRIN = 0.44V 11-bit ADC version, ADO [15:0] divided by 1000b	-0.25	0	+0.25	mV
	Resolution	12-bit ADC version, ADO [15:0] divided by 100b		±3906		Counts
	ADC Linearity Error	VRIN = 0.44V 12-bit ADC version, ADO [15:0] divided by 100b	-0.125	0	+0.125	mV

10.3 OPAMP Characteristics (VDD=3V, T_A=25℃, unless otherwise noted)

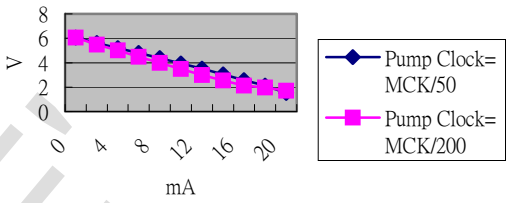
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Input Offset		-1		1	mV
	Input Offset Voltage with Chopper	Rs<100		20		V
	Input Noise Peak to Peak Voltage	Rs=100 , 0.1Hz~1Hz		1.0		Vpp
	Input Noise Peak to Peak Voltage with Chopper	Rs=100 , 0.1Hz~1Hz		0.5		Vpp
	Input Bias Current			10	30	pA
	Input Bias Current with Chopper			100	300	pA
	Input Common Mode Range		0.5		2.4	V
	Output Voltage Range		0.5		2.4	V
	Maximum Capacitor Load				50	pF

10.4 Typical Performance Characteristics

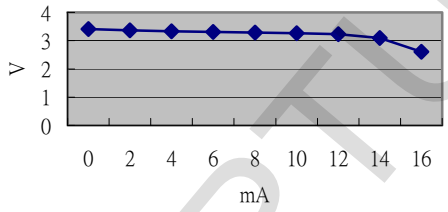
Internal Oscillator vs VDD



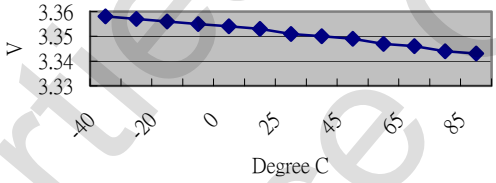
VGG vs Iout
VDD=3V, CVGG=CAB=1 μF



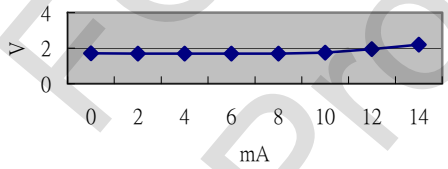
VS vs Iout
VDD=3V,CVGG=CAB=1 μF, PCK=MCK/50



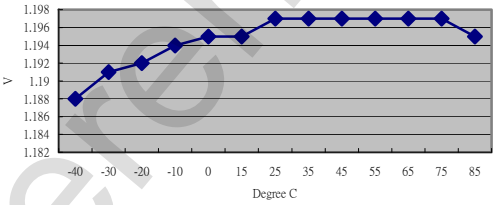
VS vs Temperature
VDD=3V, CVGG=CAB=CVDDA=1 μF, RL=1k Ohm



AGND vs Iout
VDD=3V, AGND=1/2 VDDA,
Iout=I(VDDA,AGND)



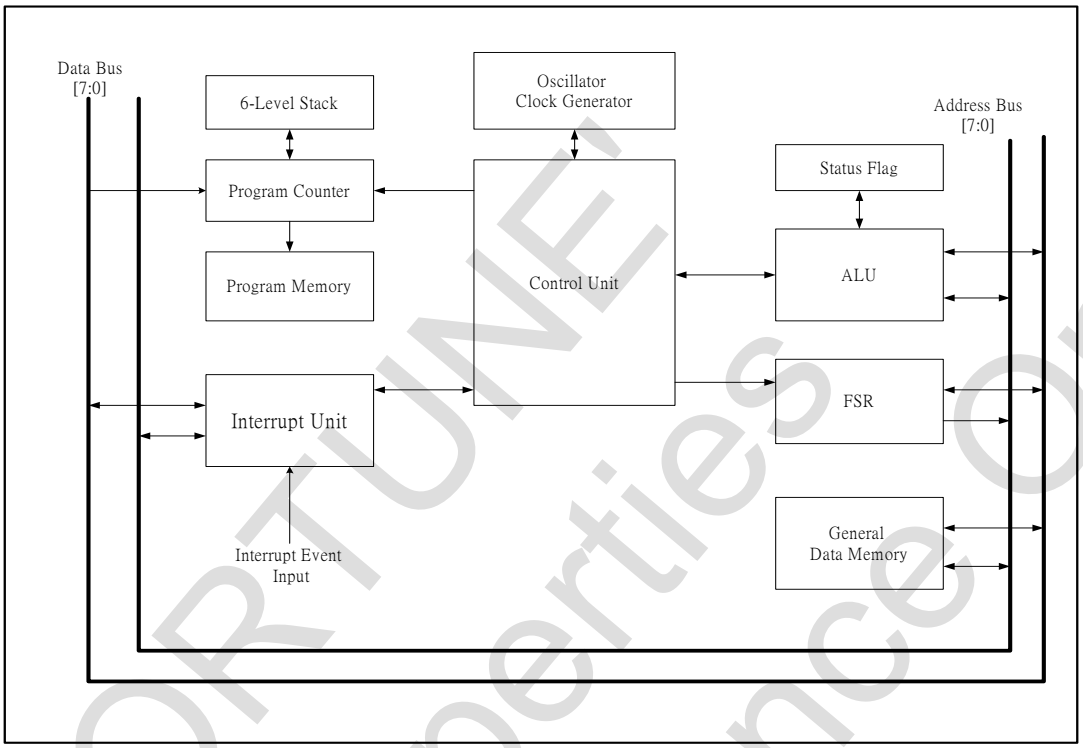
(REFO,AGND) vs Temperature
VDD=3V, R(REFO,AGND)=50k Ohm



11. Function Description

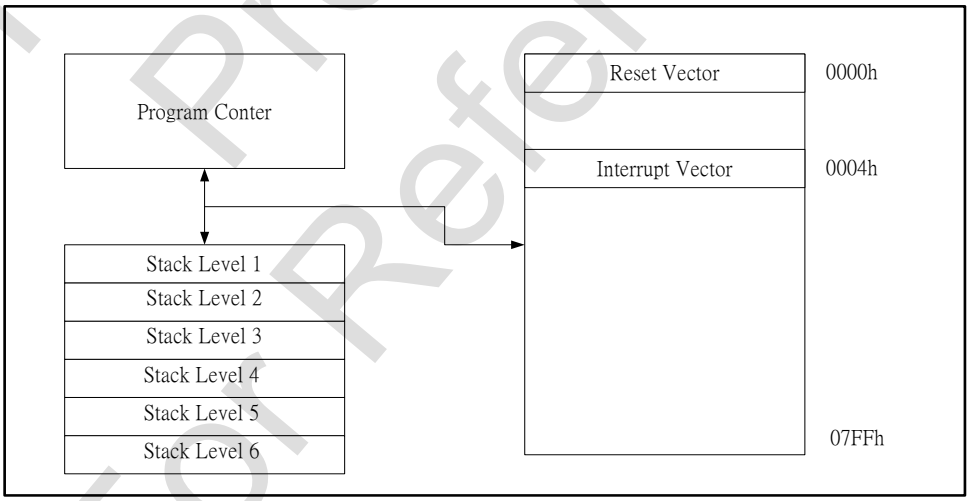
11.1 CPU Core

11.1.1 CPU Core Block Diagram



11.1.2 Program Memory Organization

FS9932 CPU has an 11-bit program counter capable of addressing a 2k x 16 program memory space. The reset vector is at 0000h and the interrupt vector is at 0004h.



11.1.3 Data Memory Organization

The data memory is partitioned into three segments. The segment with addresses 00h~07h are system special registers, like indirect address, indirect address pointer, status register, working register, interrupt flag, and interrupt control register. The segment with addresses 08h~7Fh are peripheral special registers, like I/O ports, timer, ADC, signal conditional network control register, and LCD driver. The segment with addresses 80h~FFh are general data memory.

Address	Name	Content							
00H	IND0	Use contents of FSR0 to address data memory							
01H	IND1	Use contents of FSR1 to address data memory							
02H	FSR0	Indirect data memory, address point 0							
03H	FSR1	Indirect data memory, address point 1							
04H	STATUS				PD	TO	DC	C	Z
05H	WORK	WORK register							
06H	INTF				TMIF			ADIF	E0IF
07H	INTE	GIE			TMIE			ADIE	E0IE
08h~7Fh		Peripheral special registers							
80h~FFh		General data Memory							

- IND0, IND1: indirect addressing mode address
- FSR0, FSR1: indirect addressing mode point
- PD: Power Down Flag. Cleared by writing 0 or power-on reset. Set by sleep instruction
- TO: Watch Dog Time Out Flag. Cleared by writing 0 or power-on reset. Set by Watch Dog Time Out
- DC: Digit Carry Flag, for ADDWF(C) and SUBWF(C), this bit is set if there is a carry out from the 4th order bit of resultant.
- C: Carry Flag (~Borrow)
- Z: Zero Flag
- E0IF, E0IE: PT1.0 External Interrupt flag and enable.
- ADIF, ADIE: Analog to digital converter Interrupt flag and enable.
- TMIF, TMIE: 8-bit Timer Interrupt flag and enable.
- GIE: Global interrupt enable.

11.1.4 System Special Register Description

11.1.4.1 Indirect Addressing IND0 to apply FSR0 Register

The IND0 register is not a physical register. Addressing the IND0 (00h) will cause an indirect addressing. Any instruction using the IND0 register actually accesses data pointed to by the FSR0 register.

A simple program to clear RAMS 80h-0FFh using indirect addressing is shown in following.

```
        MOVLW   080h
        MOVWF   FSR0
NEXT:   CLRF IND0
        INCFSZ  FSR0, 1
        GOTO    NEXT
```

11.4.1.2 Status Register

- C (Bit 1): R/W, Carry Flag or (~Borrow).
- Z (Bit 0): R/W, Zero Flag. Z will be set if ALU operation is zero. Reset otherwise.

Two simple examples to illustrate the relation between carry flag and arithmetic instructions.

```
Example 1
M (80h) = 3Fh   M (81h) = F0h   WORK = 99h
ADDWF   80h, 1          ; 3Fh+99h=D8h   DC=1, C=0, Z=0
ADDWF   81h, 1          ; F0h+99h=89h   DC=0, C=1, Z=0
SUBWF   80h, 1          ; 3Fh-99h=A6h   DC=1, C=0, Z=0
SUBWF   81h, 1          ; F0h-99h=57h   DC=0, C=1, Z=0
```

```
Example 2
16-bit add: {M (83h), M (82h)} = {M (83h), M (82h)} + {M (81h), M (80h)}
16-bit sub: {M (83h), M (82h)} = {M (83h), M (82h)} - {M (81h), M (80h)}
add:
        MOVFW   80h
        ADDWF   82h, 1
        MOVFW   81h
        ADDWFC  83h, 1

sub:
        MOVFW   80h
        SUBWF   82h, 1
        MOVFW   81h
        SUBWFC  83h, 1
```

11.4.1.3Interrupt Flag INTF and Interrupt enable register INTE

The interrupt enable register (INTE) records individual interrupt request. When Interrupt events occur and Interrupt enable bit =1, the interrupt flag will be set. The global interrupt enable bit (GIE) will enable CPU interrupt procedure. When GIE=1 and any interrupt flag is set, CPU interrupt procedure would be executed. CPU interrupt procedure executes GIE reset and CALL 0004h.

Note: When interrupt signal happened within instruction duty cycle, the CPU must wait and till instruction duty cycle end of this program then produce an “Interrupt Flag” before go into next step.

- This below example program is for halt and sleep mode

```
MAIN:
        HALT
        NOP
        GOTO    MAIN
MAIN_SLEEP:
        CLRFINTF
        SLEEP
        NOP
        GOTO    SYSINI
```

PS. Please make sure all interrupt flags are cleared before running SLEEP; “NOP” command must follow HALT and SLEEP commands.

11.1.5 Peripheral Special Registers

Address	Name	Content							
08H	MCK	M7_CK	M6_CK	M5_CK	M4_CK	M3_CK	M2_CK	M1_CK	M0_CK
09H	PCK					S_CHCK [1:0]		S_BEEP	S_PCK
0CH	TMOUT	TMOUT [7:0]							
0DH	TMCON	TRST	WTS [2:0]			TMEN	INS [2:0]		
10H	ADOH	ADO [15:8]							
11H	ADOL	ADO [7:0]							
13H	ADCON					ADRST	ADM [2:0]		
20H	PT1	PT1 [7:0]							
21H	PT1EN	PT1EN [7:0]							
22H	PT1PU	PT1PU [7:0]							
23H	PT1MR							E0M [1:0]	
24H	PT2	PT2 [7:6]							
25H	PT2EN	PT2EN [7:6]							
26H	PT2PU	PT2PU [7:6]							
27H	PT2MR	BPE	PWDE						
29H	NETA		SOHM						MODE
2AH	NETB	SINL [1:0]		SINH [2:0]			SFT [2:0]		
2CH	NETD							SVRL	SVRH
2EH	NETF	EN_LCDB	EN_VS	EN_VDDA	S_AGND [1:0]		EN_AGND		EN_VB
2FH	NETG						ADG [1:0]	ADEN	AZ
30H	NETH			SONE			OPEN	SOP1P [2:0]	
32H	NETJ	EN_PUMP		EN_BAND	SI_LB		EN_LB	S_LB [2:0]	
33H	NETK						LBOUT		
34H	PWDH	PWMD [15:8]							
35H	PWDL	PWMD [7:0]							
36H	PWCON					PWEN		PWCS [2:0]	
40H	LCD1	SEG1 [3:0]					SEG0 [3:0]		
42H	PT5O								PT5 [1:0]
43H	PT6O								PT6 [1:0]
4CH	LCD6	SEG11 [3:0]					SEG10 [3:0]		
50H	LCD5	SEG9 [3:0]					SEG8 [3:0]		
51H	LCD4	SEG7 [3:0]					SEG6 [3:0]		
52H	LCD3	SEG5 [3:0]					SEG4 [3:0]		
53H	LCD2	SEG3 [3:0]					SEG2 [3:0]		
54H	LCDENR	LCDCKS [1:0]		LCDEN			S_LCDO [1:0]		

11.1.6 Instruction Set

Instruction	Operation	Cycle	Flag
NOP	No operation	1	None
CLRF f	f = 0	1	Z
ADDWF f, d	d = f + W	1	C, DC, Z
INCF f, d	d = f + 1	1	Z
INCFSZ f, d	d = f + 1 skip if d = 0	1, 2	None
DECF f, d	d = f - 1	1	Z
DECFSZ f, d	d= f - 1 skip if d = 0	1, 2	None
SUBWF f, d	d = f - W	1	C, DC, Z
COMF f, d	d = ~f	1	Z
MOVWF f	f = W	1	None
MOVFW f	W = f	1	None
ADDWFC f, d	d = f + W + C	1	C, DC, Z
ANDWF f, d	d = f & W	1	Z
IORWF f, d	d = f | W	1	Z
XORWF f, d	d = f ^ W	1	Z
RLF f, d	C, d [7:0] = f [7:0], C	1	C,Z
SUBWFC f, d	d = f - W - (~C)	1	C, DC, Z
RRF f, d	d [7:0], C = C, f [7:0]	1	C, Z
ADDLW k	W = k + W	1	C, DC, Z
SUBLW k	W = k - W	1	C, DC, Z
ANDLW k	W = k & W	1	Z
IORLW k	W = k | W	1	Z
XORLW k	W = k ^ W	1	Z
MOVLW k	W = k	1	None
RETLW k	RETURN and W = k	2	None
CALL k	Push PC + 1 and GOTO k	2	None
GOTO k	PC = k	2	None
RETFIE	Pop PC and GIE = 1	2	None
RETURN	Pop PC	2	None
HALT	Stop MCU clock	1	None
SLEEP	Stop OSC	1	PD
CLRWDT	Clear watch dog timer	1	None
ADDPCW	PC = PC + 1 + {6{W [7], W [6:0]}	2	None
BCF f, b	f [b] = 0	1	None
BSF f, b	f [b] = 1	1	None
BTFSC f, b	Skip if f[b] = 0	1, 2	None
BTFSS f, b	Skip if f[b] = 1	1, 2	None

- f: memory address (0h ~ FFh).
- W: work register.
- k: literal field, constant data or label.
- d: destination select: d=0 store result in W, d=1: store result in memory address f.
- b: bit select (0~7).
- M (f): the content of memory address f.
- PC: program counter.

11.1.7 Instruction Description

NOP	**No Operation**
Syntax	NOP
Operation	No Operation
Status Affected	None
Description	No operation. NOP is used for one instruction cycle delay.

CLRF	**Clear f**
Syntax	CLRFf
Operation	0 => M (f)
Status Affected	1=> Z
Description	Reset memory address f content.

ADDWF	**Add W to f**
Syntax	ADDWF f, d
Operation	W + M (f) => (destination)
Status Affected	DC, C, Z
Description	Add the content of the W register and M (f). If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

INCF	**Increment f**
Syntax	INCF f, d
Operation	M (f) + 1 => (destination)
Status Affected	Z
Description	M (f) is incremented. If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

INCFSZ	**Increment f, skip if zero**
Syntax	INCFSZ f, d
Operation	M (f) + 1 => (destination), skip if result is zero
Status Affected	None
Description	M (f) is incremented. If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f). If the result is 0, then the next fetched instruction is discarded and a NOP is executed instead making it a two-cycle instruction.

DECF	**Decrement f**
Syntax	DECF f, d
Operation	M (f) - 1 => (destination)
Status Affected	Z
Description	M (f) is decremented. If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

DECFSZ	**Decrement f, skip if zero**
Syntax	DECFSZ f, d
Operation	M (f) - 1 => (destination), skip if result is zero
Status Affected	None
Description	M (f) is decremented. If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f). If the result is 0, then the next fetched instruction is discarded and a NOP is executed instead making it a two-cycle instruction.

SUBWF	**Subtract W from f**
Syntax	SUBWF f, d
Operation	M (f) + NOT (W) + 1 => (destination)
Status Affected	DC, C, Z
Description	Subtract the content of the W register from M (f). If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f),

COMF	Complement f
Syntax	COMF f, d
Operation	NOT (M (f)) => M (f)
Status Affected	Z
Description	M (f) is complemented. If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f)

MOVWF	Move W to f
Syntax	MOVWF f
Operation	W => M (f)
Status Affected	None
Description	Move data from the W register to M (f).

MOVFW	Move f to W
Syntax	MOVFW f
Operation	M (f) => W
Status Affected	None
Description	Move data from M (f) to the W register.

ADDWFC	Add W, f and Carry
Syntax	ADDWFC f, d
Operation	W + M (f) + C => (destination)
Status Affected	DC, C, Z
Description	Add the content of the W register, M (f) and Carry bit. If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

ANDWF	And W and f
Syntax	ANDWF f, d
Operation	W AND M (f) => (destination)
Status Affected	Z
Description	AND the content of the W register with M (f). If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

IORWF	Inclusive OR W and f
Syntax	IORWF f, d
Operation	W OR M (f) => (destination)
Status Affected	Z
Description	Inclusive OR the content of the W register and M (f). If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

XORWF	Exclusive OR W and f
Syntax	XORWF f, d
Operation	W XOR M (f) => (destination)
Status Affected	Z
Description	Exclusive OR the content of the W register and M (f). If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

RLF	Rotate left M (f) through Carry
Syntax	RLF f, d
Operation	M (f) [6:0], C => (destination)
Status Affected	C, Z
Description	M (f) is rotated one bit to the left through the Carry bit. If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

SUBWFC	Subtract W and Carry from f
Syntax	SUBWFC f, d
Operation	M (f) + NOT (W) + C => (destination)
Status Affected	DC, C, Z
Description	Subtract the content of the W register from M (f). If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

RRF	Rotate right M (f) through Carry
Syntax	RRF f, d
Operation	C, M (f) [7:1] => (destination)
Status Affected	C
Description	M (f) is rotated one bit to the right through the Carry bit. If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

ADDLW	ADD literal to W
Syntax	ADDLW k
Operation	W + k => W
Status Affected	DC, C, Z
Description	Add the content of the W register and the eight-bit literal "k". The result is stored in the W register.

SUBLW	Subtract literal from W
Syntax	SUBLW k
Operation	k + NOT (W) + 1 => W
Status Affected	DC, C, Z
Description	Subtract the eight-bit literal "k" from the content of the W register. The result is stored in the W register.

ANDLW	AND literal with W
Syntax	ANDLW k
Operation	W AND k => W
Status Affected	Z
Description	AND the content of the W register with the eight-bit literal "k". The result is stored in the W register.

IORLW	Inclusive OR literal with W
Syntax	IORLW k
Operation	W OR k => W
Status Affected	Z
Description	Inclusive OR the content of the W register and the eight-bit literal "k". The result is stored in the W register.

XORLW	Exclusive OR literal with W
Syntax	XORLW k
Operation	W XOR k => W
Status Affected	Z
Description	Exclusive OR the content of the W register and the eight-bit literal "k". The result is stored in the W register.

MOVLW	Move literal to W
Syntax	MOVLW k
Operation	k => W
Status Affected	None
Description	Move the eight-bit literal "k" to the content of the W register.

RETLW	Return and move literal to W
Syntax	RETLW k
Operation	k => W [Top Stack] => PC Pop Stack
Status Affected	None
Description	Move the eight-bit literal "k" to the content of the W register. The program counter is loaded from the top stack, then pop stack.

CALL	Subroutine CALL
Syntax	CALL k
Operation	Push Stack PC + 1 => [Top Stack] k => PC
Status Affected	None
Description	Subroutine Call. First, return address PC + 1 is pushed onto the stack. The immediate address is loaded into PC.

GOTO	Unconditional Branch
Syntax	GOTO k
Operation	k => PC
Status Affected	None
Description	The immediate address is loaded into PC.

Return	Return from Subroutine
Syntax	RETURN
Operation	[Top Stack] => PC Pop Stack
Status Affected	None
Description	The program counter is loaded from the top stack, then pop stack.

RETFIE	Return from Interrupt
Syntax	RETFIE
Operation	[Top Stack] => PC Pop Stack 1 => GIE
Status Affected	None
Description	The program counter is loaded from the top stack, then pop stack. Setting the GIE bit enables interrupts.

ADDPCW	ADD W to Program Counter
Syntax	ADDPCW
Operation	PC + 1 + W => PC
Status Affected	None
Description	The relative address PC + 1 + W is loaded into PC. The working register must less than 80h (128d).

HALT	Stop CPU Core Clock
Syntax	HALT
Operation	CPU Stop
Status Affected	None
Description	CPU clock is stopped. Oscillator is running. CPU can be waked up by internal and external interrupt sources.

SLEEP	Oscillator stop
Syntax	SLEEP
Operation	CPU oscillator is stopped
Status Affected	PD
Description	CPU oscillator is stopped. CPU can be waked up by external interrupt sources.

PS. Please make sure all interrupt flags are cleared before running SLEEP; "NOP" command must follow HALT and SLEEP commands.

CLRWDT	**Clear watch dog timer counter**
Syntax	CLRWDT
Operation	Watch dog timer counter will reset
Status Affected	None
Description	CLRWDT instruction will reset watch dog timer counter.

BSF	**Bit Set f**
Syntax	BSF f, b
Operation	1 => M (f) [b]
Status Affected	None
Description	Bit b in M (f) is set to 1.

BCF	**Bit Clear f**
Syntax	BCF f, b
Operation	0 => M (f) [b]
Status Affected	None
Description	Bit b in M (f) is reset to 0.

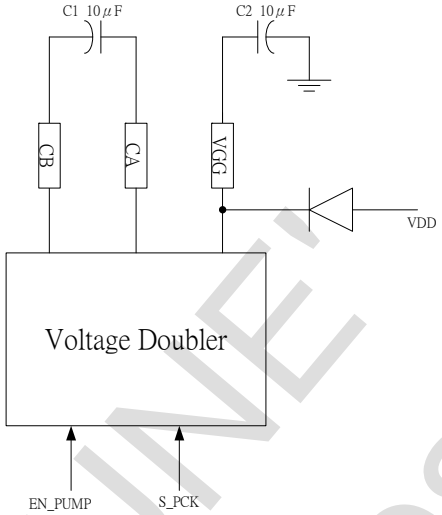
BTFSC	**Bit Test skip if Clear**
Syntax	BTFSC f, b
Operation	Skip if M (f) [b] = 0
Status Affected	None
Description	If bit 'b' in M (f) is 0, the next fetched instruction is discarded and a NOP is executed instead making it a two-cycle instruction.

BTFSS	**Bit Test skip if Set**
Syntax	BTFSS f, b
Operation	Skip if M (f) [b] = 1
Status Affected	None
Description	If bit 'b' in M (f) is 1, the next fetched instruction is discarded and a NOP is executed instead making it a two-cycle instruction.

11.2 Power System

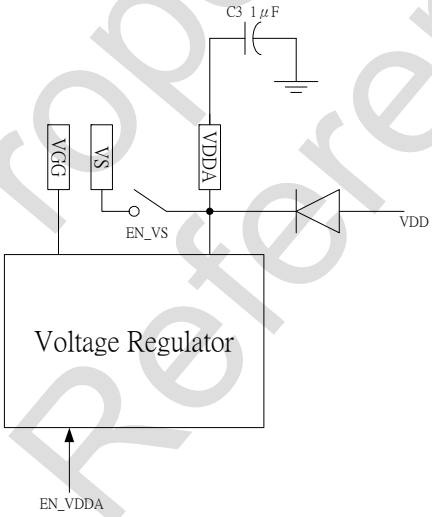
Address	**Name**	**Content**							
2EH	NETF	EN_LCDB	EN_VS	EN_VDDA	S_AGND [1:0]		EN_AGND		EN_VB
32H	NETJ	EN_PUMP		EN_BAND	SI_LB	EN_LB	S_LB [2:0]		
33H	NETK					LBOUT			

11.2.1 Voltage Doubler



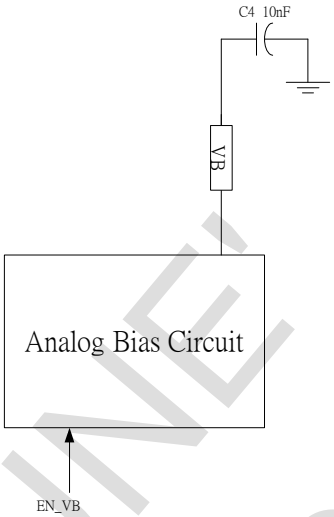
- When EN_PUMP=1, voltage doubler is enabled. The VGG voltage is about two times VDD. When EN_PUMP=0, you can input a voltage as voltage regulator power supply.
- Voltage doubler operation frequency is selected by S_PCK. The details are described in the section “clock system”.
- Typical values for C1 and C2 are 1μF~10μF. For large load current, larger capacitors should be used to reduce the output voltage ripple. If a polarity capacitor is used for C1, the CB pin should be connected to the negative terminal of the capacitor, and the CA pin to the positive terminal.

11.2.2 Voltage Regulator



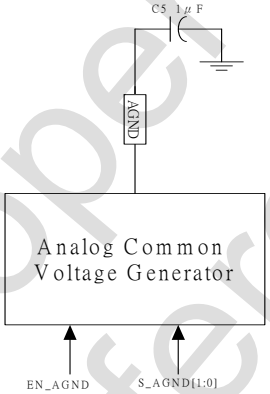
- VDDA is the power supply voltage for analog circuit and LCD driver. When EN_VDDA is set, the voltage regulator will be enabled. Otherwise VDDA can be used as external regulated power supply input.
- The typical capacitance for C3 is 1μF~10μF. For large load current, large capacitor should be used to increase the output voltage stability.

11.2.3 Analog Bias Circuit



- Prior to enabling the analog block, EN_VB must be set. When the internal voltage doubler is used, a 10nF capacitor must be connected between Pin VB and VSS for reducing voltage doubler's noise.

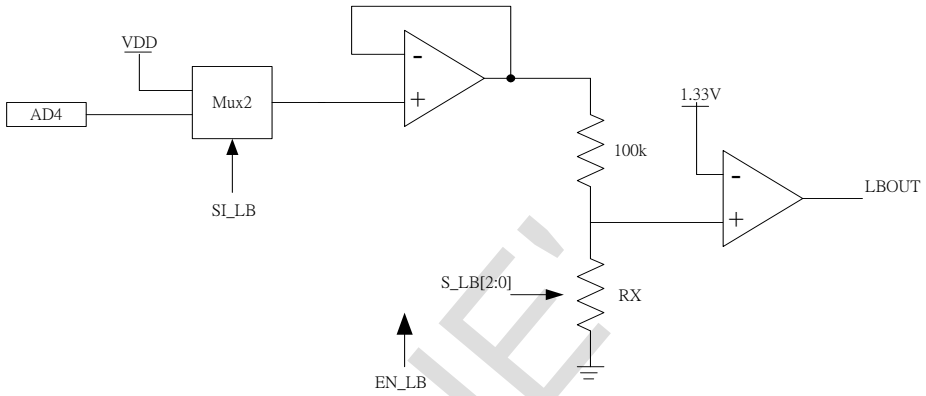
11.2.4 Analog Common Voltage Generator



- AGND is analog common voltage. When EN_AGND=1, analog common voltage generator is enabled.
- S_AGND: select AGND Voltage. In general, the mode of 1/2 VDDA is used.

S_AGND [1:0]	AGND Voltage
00	1/4 VDDA
01	1/2 VDDA
10	1/3 VDDA
11	2/3 VDDA

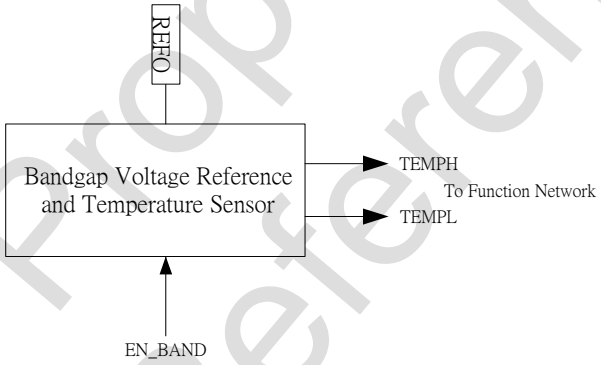
11.2.5 Low Battery Comparator



- When EN_LB=1, low battery comparator is enabled.
- When SI_LB=0, OPAMP input is VDD. Otherwise OPAMP input is external pin AD4 (PT1.1).
- S_LB [2:0] is used to select the resistance of RX.

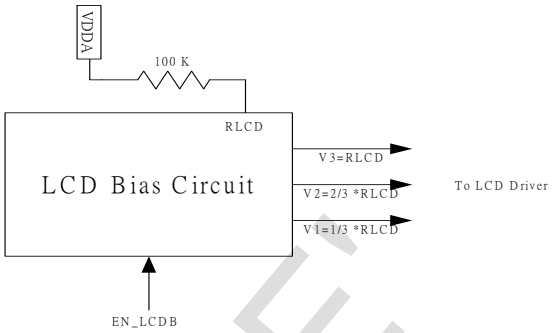
S_LB [2:0]	RX	Low Battery Voltage
000	90k	2.1
001	97k	2.2
010	104k	2.3
011	124k	2.4
100	134k	2.5
101	149k	2.6
110	164k	2.7
111	184k	2.8

11.2.6 Bandgap Voltage and Temperature Sensor



- REFO is low temperature coefficient bandgap voltage reference output. When EN_BAND=1, the circuit is enabled. The output voltage to AGND is about 1.2V. Typical temperature coefficient is 100ppm/°C.
- {TEMPH, TEMPL} is proportional to ambient temperature. They can be connected to ADC input and converted to digital numbers (typical 530μV±50μV/°C).

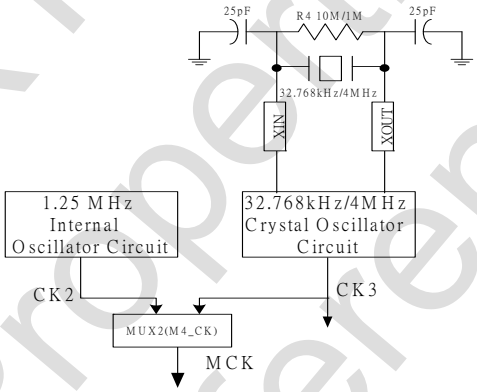
11.2.7 LCD Bias Circuit



- V3, V2, V1 are the output voltages of Bias Circuit. The voltages to VSS are about RLCD, 2/3 RLCD and 1/3 RLCD. When EN_LCDB=1, the circuit is enabled.

11.3 Clock System

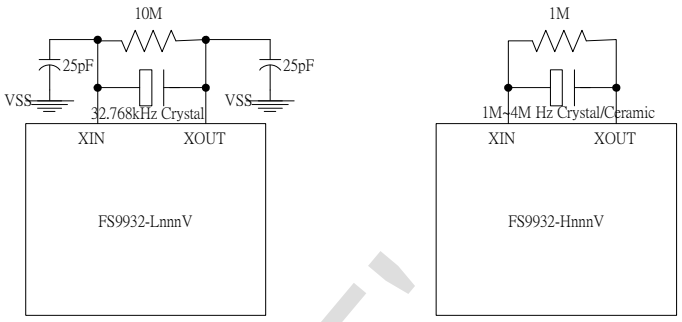
Address	Name	Content							
08H	MCK	M7_CK	M6_CK	M5_CK	M4_CK		M2_CK	M1_CK	M0_CK
09H	PCK					S_CHCK [1:0]		S_BEEP	S_PCK



11.3.1 Oscillator State

Input			Oscillator State	
Sleep	M7_CK	M6_CK	CK2	CK3
1	X	X	Disable	Disable
0	0	0	Enable	Enable
0	0	1	Enable	Disable
0	1	0	Disable	Enable
0	1	1	Disable	Disable

- External oscillator can use 32768Hz crystal or 1~4MHz crystal/ceramic, as shown in the following Figures. To order Mask Code please use FS9932-LnnnV for 32768Hz crystal, FS9932-HnnnV for 1~4MHz crystal/ceramic.



- When using FS9932F_ICE Chip, there are two sets of external pins for Oscillator Circuit: XIN1 and XOUT1 for 32768Hz crystal, XIN2 and XOUT2 for 1~4MHz crystal/ceramic. For the unused pin set, the external circuits should be removed and pins XIN1 (or XIN2) should be connected to VDD.
- When the external oscillator is disabled then restarted, the oscillator need to wait for a period of time before it can start. The typical waiting time for 32768Hz crystal oscillator is about 1s.
- When disabling an oscillator, it is necessary to make sure that the oscillator is not disabled during CPU operation clock cycle.
- M4_CK=”0”, MCK=CK2; M4_CK=”1”, MCK=CK3/2.

11.3.2 CPU Instruction Cycle

M2_CK	M1_CK	M0_CK	Instruction Cycle
X	X	1	CK3/8
1	1	0	MCK/4
1	0	0	MCK/8
0	1	0	MCK/12.5
0	0	0	MCK/25

- When M2_CK=0, CPU has a different operation clock cycle from ADC in order to maintain a stable ADC output. In applications where a resolution of more than 13-bits is necessary, M2_CK should be set to zero.
- CPU’s operation clock cycle may change as M0_CK, M1_CK, M2_CK, M4_CK change. Users must make sure that switching can be made only after the oscillator’s output is stabilized. An NOP command should be added after the switching.

```
BSF   MCK, 2
NOP
…
```

- Below are some example programs to change CPU instruction cycle.

Example 1
Set the instruction cycle time to 2μs.

MCK/4 as external crystal oscillator is 4MHz

```
MOVLW     10x1x110b  ; x: Don't care
MOVWF     MCK
NOP
…
```

Example 2
Set the instruction cycle time to 4μs.

MCK/8 as external crystal oscillator is 4MHz

```
MOVLW     10x1x100b  ; x: Don't care
MOVWF     MCK
NOP
…
```

Example 3 Set the instruction cycle time to 3.2μs. MCK/4 as internal crystal oscillator is 1.25MHz
MOVLW 01x0x110b ; x: Don't care MOVWF MCK NOP …

Example 4 Set the instruction cycle time to 6.4μs. MCK/8 as internal crystal oscillator is 1.25MHz
MOVLW 01x0x100b ; x: Don't care MOVWF MCK NOP …

11.3.3 ADC Sample Frequency

M1_CK	ADC sample Frequency (ADCF)
0	MCK/50
1	MCK/25

■ ADC sampling frequency should be set between 40 kHz and 80kHz in order to get a better characteristic.

11.3.4 Beeper Clock

M0_CK	S_BEEP	Beeper Clock
0	1	MCK/500
0	0	MCK/750
1	X	CK3/8

11.3.5 Voltage Doubler Operation Frequency

M0_CK	S_PCK	Voltage Doubler's Operation Frequency
0	1	MCK/50
0	0	MCK/200
1	X	CK3/32

11.3.6 Chopper Operation Amplifier Input Control Signal

S_CHCK [1]	S_CHCK [0]	Chopper Control Signal
0	0	0
0	1	1
1	0	MCK/1000
1	1	MCK/2000

11.3.7 Timer and LCD Module Input Clock

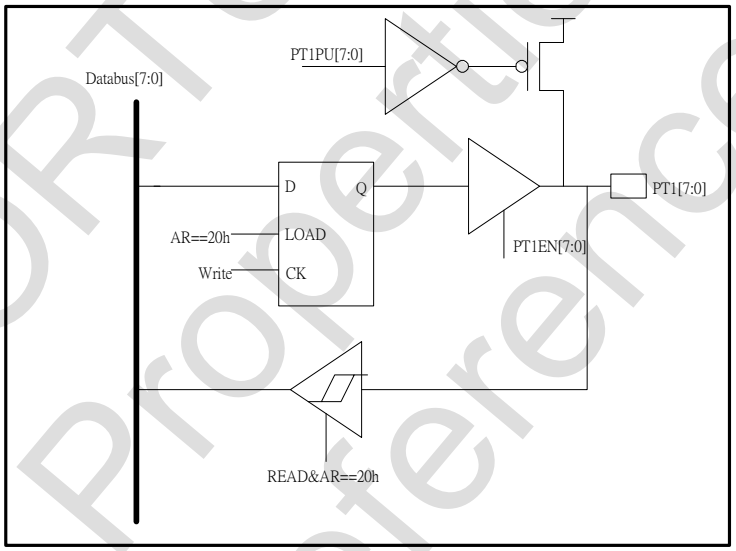
M5_CK	Timer and LCD Module input Clock TMCLK
0	MCK/2000
1	CK3/32

11.4 I/O Port

11.4.1 PT1

Address	Name	Content							
06H	INTF								E0IF
07H	INTE	GIE							E0IE
20H	PT1	PT1 [7:0]							
21H	PT1EN	PT1EN [7:0]							
22H	PT1PU	PT1PU [7:0]							
23H	PT1MR							E0M [1:0]	

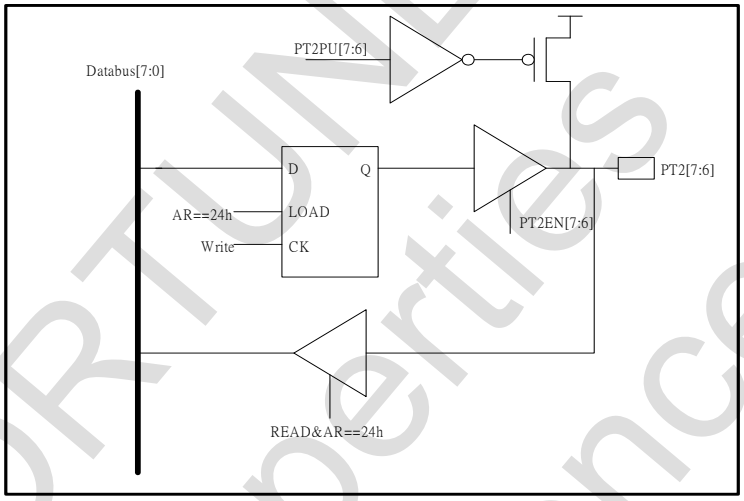
- PT1 is I/O port with pull-up resistor enable control.
- PT1 [N] is an input port when PT1EN [N] =”0”, PT1 [N] is an output port when PT1EN [N] is “1”; system reset is “0”.
- When PT1PU [N]=”0”, PT1 [N] has no pull-up resistor; When PT1PU[N]=“1”, PT1 [N] has a pull-up resistor; system reset is “0”.
- PT1 [0] can be used as an external interrupt source. Interrupt mode is controlled by E0M [1:0]: ”00” for negative edge, “01” for positive edge, “10”&”11”for interrupt during other time.
- PT1 has Schmitt-trigger input.
- PT1.1 can be ADC channel “AD4”, PT1.2 can be ADC channel “AD5”.



11.4.2 PT2

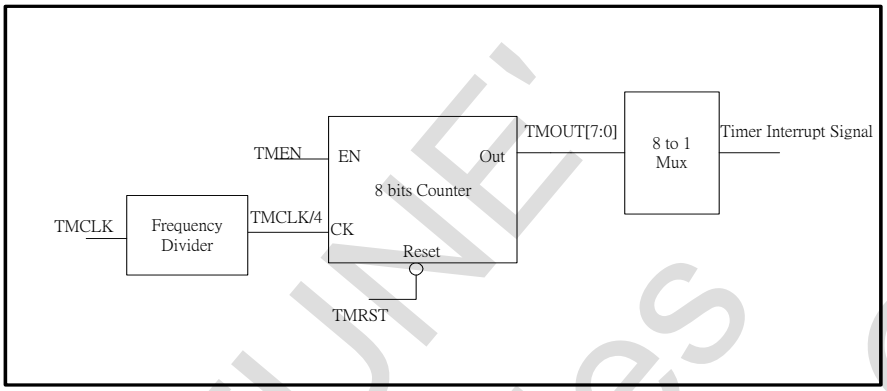
Address	Name	Content							
24H	PT2	PT2 [7:6]							
25H	PT2EN	PT2EN [7:6]							
26H	PT2PU	PT2PU [7:6]							
27H	PT2MR	BPE	PWDE						

- PT2 is an I/O port with pull-up resistor enabling control.
- When PT2EN [N] =”0”, PT2 [N] is an input port; When PT2EN [N]= “1”, PT2 [N] is an output port. System reset is “0”.
- When PT2EN [7]=”1”, PT2 [7] is used as buzzer output. BPE=”1”.
- When PWDE=”1” and PT2EN [6]=”1”, PT2.6 is PDM Output.



11.5 8-Bit Timer

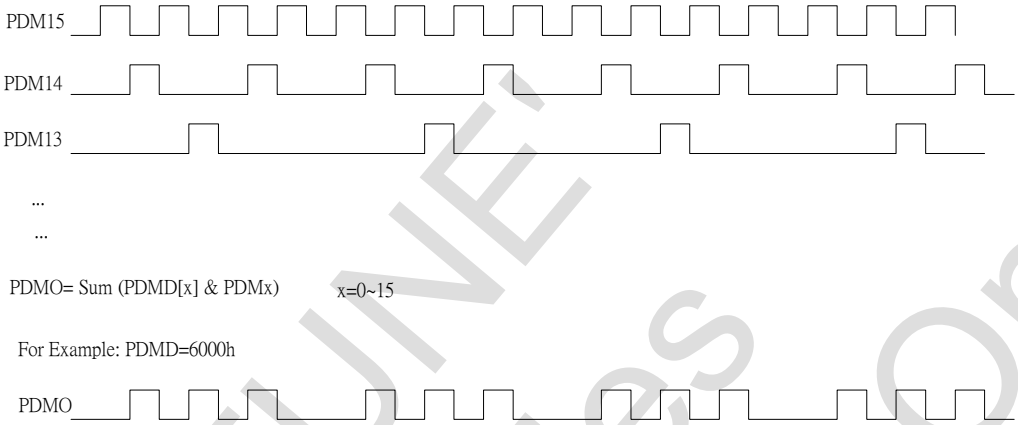
Address	Name	Content							
06H	INTF				TMIE				
07H	INTE	GIE			TMIF				
0CH	TMOUT	TMOUT [7:0]							
0DH	TMCON	TRST				TMEN	INS [2:0]		



- After writing a “0” to bit 7 of address 0Dh, the CPU will send a low pulse to TRST and reset the 8-bit counter. Then read bit 7 of 0DH to get “1”.
- When TMEN=1, the 8-bit counter is enabled. When TMEN=0, the 8-bit counter stops.
- NS [2:0] selects timer interrupt source. The selection codes are as follows: 000 for TMOUT [0], 001 for TMOUT [1], 010 for TMOUT [2], 011 for TMOUT [3], 100 for TMOUT [4], 101 for TMOUT [5], 110 for TMOUT [6], 111 for TMOUT [7].
- TMOUT [7:0] is the output of the 8-bit counter. It is read-only.

11.6 PDM (Pulse Density Modulator) Module

Address	Name	Content					
34H	PWDH	PDMD [15:8]					
35H	PWDL	PDMD [7:0]					
36H	PWCON				PDEN		PDCS [2:0]

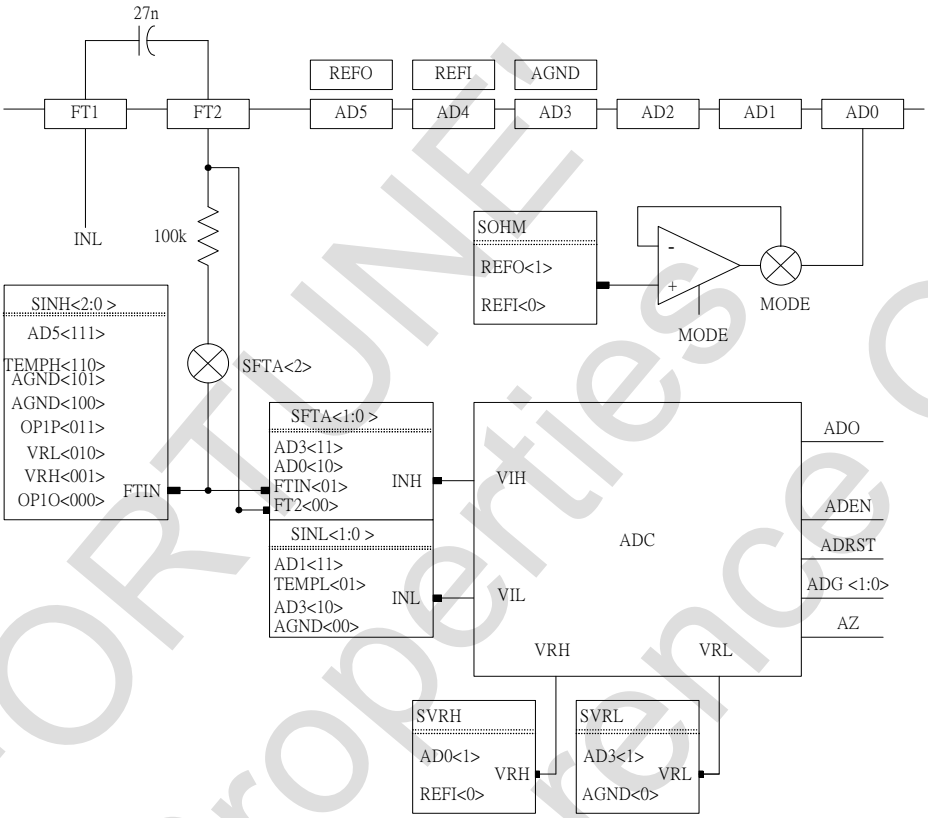


- PDEN: Enable PDM Module.
- PDCS: Select Input Frequency.

PDCS	PDM Pulse Width
000	1/MCK
001	2/MCK
010	4/MCK
011	8/MCK
100	16/MCK
101	32/MCK
110	64/MCK
111	128/MCK

11.7 ADC Input Multiplexer and Low Pass Filter

Address	Name	Content							
29H	NETA		SOHM						MODE
2AH	NETB	SINL [1:0]		SINH [2:0]			SFT [2:0]		
2CH	NETD							SVRL	SVRH



11.7.1 ADC Pre-filter

The input signal is sampled by the ADC. When the input signal has a noise with frequency higher than the sampling frequency, the noise generates low frequency noises through sampling circuit. Hence it is recommended to pass the input signal through a low pass filter, in order to get a stable ADC output.

FS9932 has an internal 100k ohm resistor, which is for the construction of a low pass filter through parallel connection with an external capacitor between two pins FT1 and FT2. The capacitance is normally between 10nF and 50nF. Please note that a larger capacitance may cause too much time delay in input signal switching. SFT<2> decides if an input signal passes the low pass filter. SFTA<1:0> decides whether the ADC's input is through a low pass filter, or direct input, or through AD3 and AD0.

11.7.2 ADC Input Multiplexers

The positive and negative input terminals of ADC and reference voltages can be selected by analog multiplexers and set to status specified by users. The ones of the ADC can also be set by SINH<2:0>, and SFTA<1:0>. The input OP1P terminal of SINH multiplexer can be selected by SOP1P<2:0>.

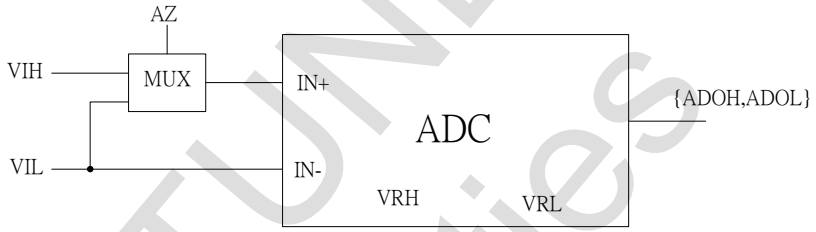
When measuring internal temperature, the positive terminal of ADC should be connected to TEMPH, and the negative one connected to TEMPL. The reference voltage is fixed and around 0.4V.

11.7.3 AD0 Voltage Source

When MODE=1, ADO can be used as voltage source. Its voltage is selected by SOHM as REFO or REFI voltage. The output current is less than 500uA.

11.8 ADC Control Register

Address	Name	Content							
06H	INTF							ADIF	
07H	INTE	GIE						ADIE	
10H	ADOH	ADO [15:8]							
11H	ADOL	ADO [7:0]							
13H	ADCON					ADRST	ADM [2:0]		
2FH	NETG					ADG [1:0]		ADEN	AZ



- The ADC (analog to digital converter) contains S-D modulator and digital comb filter. When ADRST=1, comb filter will be enabled. When ADRST=0, the comb filter will be reset. ADEN=1 starts the S-D modulator.
- The output rate is selected by ADM (N).

ADM (N)	ADC Output Rate
000	ADCF/125
001	ADCF/250
010	ADCF/500
011	ADCF/1000
100	ADCF/2000
101	ADCF/4000
110	ADCF/8000
111	ADCF/8000

- AZ=0 means that the ADC's differential inputs are (VIH, VIL); AZ= 1 means that the ADC differential inputs are (VIL, VIL). We can use this mode to measure the ADC offset.
- ADG [1:0] will set ADC's input gain as follows: 00 for 2/3, 01 for 1, 10 for 2, and 11 for 2 1/3.

11.9 ADC Application Guide

The ADC used in FS9932 is a Σ-Δ ADC with fully differential inputs and fully differential reference voltage inputs. Its maximum output is ±15625.

The conversion equation is: Dout = 15625 * G * (VIH – VIL + Vio) / (VRH – VRL + Vro).

VIH is ADC's positive input voltage. VIL is ADC's negative input voltage. Vio is ADC's offset on the input terminals. VRH is the voltage at the positive input of Reference Voltage. VRL is the voltage at the negative input of Reference Voltage. Vro is the offset on the input terminals of Reference Voltage. And (VRH – VRL + Vro) > 0. When G * (VIH – VIL + Vio) / (VRH – VRL + Vro) ≧ 1, Dout = 15625. When G * (VIH – VIL + Vio) / (VRH – VRL + Vro) ≦ -1, Dout = -15625.

11.9.1 ADC Output Format

CPU can read {ADOH,ADOL} as ADC's 16-bit output. Note that the output is in 2's complement format, i.e., "1" in the most significant bit (MSB) denotes a negative number. For example, if {ADOH, ADOL} = E2F7h, then Dout = -(not(E2F7h) + 1) = -7433.

11.9.2 ADC Linear Range

Σ-Δ ADC is close to saturation when G * (VIH – VIL + Vio) / (VRH – VRL + Vro) is close to ±1, and has good linearity in the range of ± 0.95.

11.9.3 ADC Output Rate and Settling Time

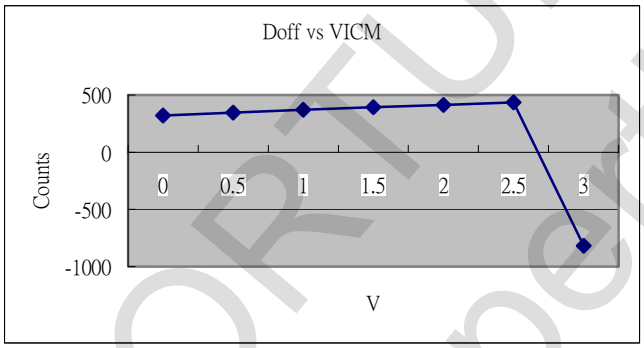
Σ-Δ ADC is generally an over-sampling ADC. Every ADC output is the result of sampling N times and processed by DSP. FS9932 ADC's sampling frequency is decided by M1_CK. ADCM decides to send out a 16-bit value after sampling N times, and an interrupt signal every time the ADC outputs the value. In fact, every ADC output includes previous 2*N times sampling results. If ADC's input, reference voltage, ADG or AZ is switched, the previous two outputs are normally not stable ones, the third output and beyond are stable.

11.9.4 ADC Input Offset

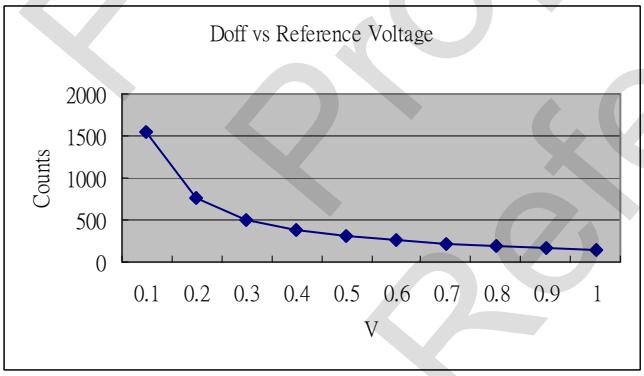
ADC Input Offset Vio drifts with temperature and common mode voltage at the inputs. When the drifting is slow, set AZ bit to 1, and Doff = 15625 * G * (Vio) / (VRH – VRL + Vro).

When measuring, Doff should be deducted. The relationships of Doff with voltage inputs of common mode and reference voltage are shown as follows.

- (VRH, AGND) = 0.4V, VRL = AGND, VIH = VIL = VICM, ADG = 01.



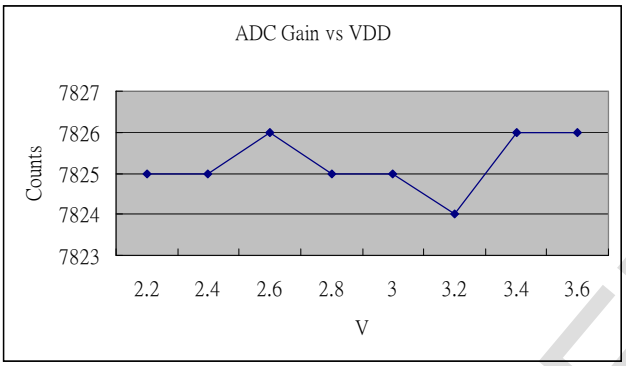
- (VRH, AGND) = 0.5V~1V, VRL = AGND, VIH = VIL = AGND, ADG = 01.



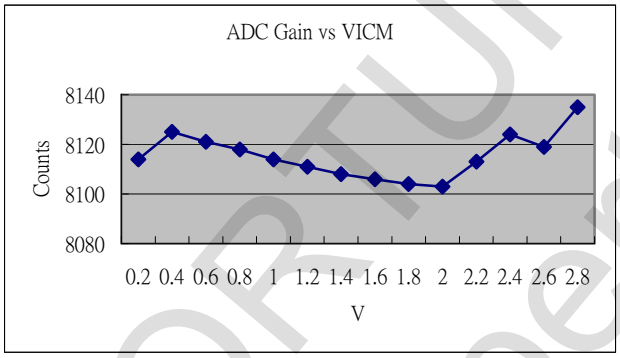
11.9.5 ADC Gain

ADC output deducted by Doff is ADC Gain. Within ADC operation range, the changes of ADC Gain are shown as follows. The results show that ADC Gain does not change as VDD changes. The suggested values for common mode voltages at ADC input and reference voltage are 1V~2V.

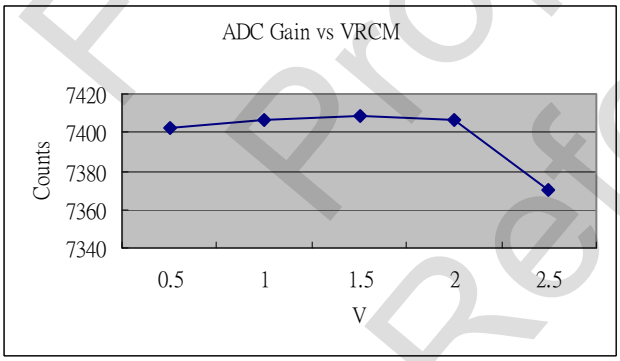
- ADC Gain vs. VDD: (VRH, VRL) = 1/3 * (REFO, AGND), (VIH, VIL) = 1/6 * (REFO, AGND), VRL = VIL = AGND, ADG = 01, VDD = 2.2V~3.6V.



- ADC Gain vs. Voltage Inputs of Common Mode: (VRH, VRL) = 1/3 * (REFO, AGND), (VIH, VIL) = 0.2V, VRL = AGND, VICM = 1/2 * (VIH+VIL), ADG = 01.



- ADC Gain vs. Voltage Reference of Common Mode: (VRH, VRL) = 0.4, (VIH, VIL) = 1/6 * (REFO, AGND), VRCM = 1/2 * (VRL + VRH), VIL = AGND, ADG = 01.



11.9.6 ADC Resolution

ADC resolution is mainly decided by ADCM (ADC output rate) and reference voltage, and the results are as follows:

- (VRH, VRL) = 0.4V, (VIH, VIL)= 0.2V, VRL = VIL = AGND, G=1.

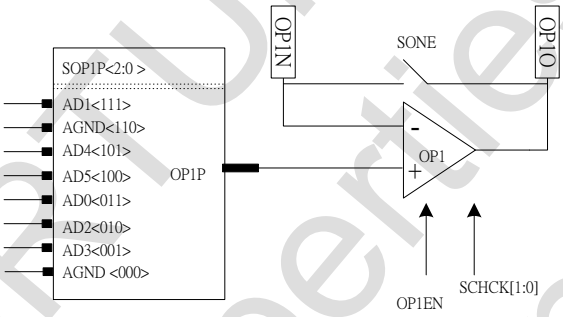
ADM	000	001	010	011	100	101	110
Rolling counts	10	6	4	3	3	2	1

- (VRH, VRL) = VR, (VIH, VIL) = 1/2 * VR, VRL = VIL = AGND, G = 1, ADM = 101.

VR	**0.05**	**0.1**	**0.2**	**0.3**	**0.4**	**0.6**	**0.8**	**1.0**
Rolling counts	31	15	5	3	2	2	4	9

11.10 OPAMP Control Register

Address	**Name**	**Content**							
30H	NETH			SONE		OPEN	SOP1P [2:0]		
09H	PCK					S_CHCK [1:0]			



- ENOP is the OPAMP enable control signal.
- When SONE = 1, the output and negative input of OPAMP is short, and OPAMP becomes a unit-gain buffer.
- S_CHCK [1:0], OP1 input operation mode can be set as: 00 for +Offset, 01 for -Offset, 10 for MCK/1000 chopper frequency, and 11 for MCK/2000 chopper frequency.

11.11 Low Noise Operation Amplifier Guide

The input noise of CMOS OPAMP is generally much larger than the one of Bipolar OPAMP. Moreover, the flick noise (1/f noise) of CMOS is a killer for low frequency small signal measurement. But the need for input bias current in Bipolar OPAMP causes that some transducers can't be used. In general, Bipolar process is not good for highly integrated ICs. FS9932 used special CMOS low noise circuit design, and under normal conditions, the input noise is controlled under 1μVpp (0.1Hz~1Hz). FS9932 is good for transducer applications because there is no need to consider input bias current.

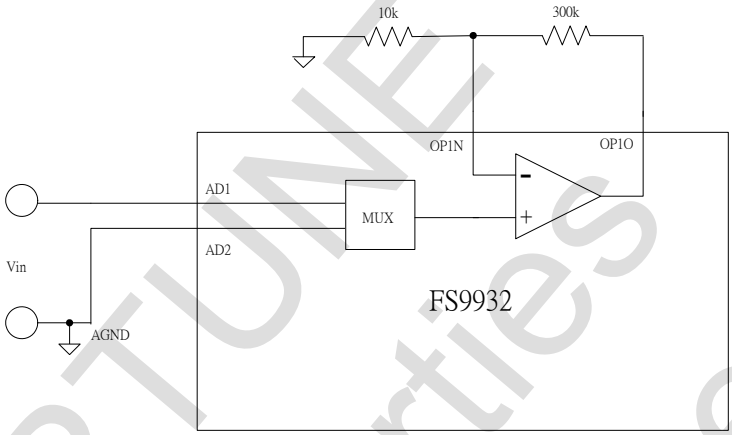
Most of the input noise in CMOS OPAMP comes from input differential amplification. S_CHCK can be set to switch the differential amplification: 00 for positive offset voltage, 01 for negative offset voltage. Using one clock pulse to switch input differential amplification is called chopper mode. In general, chopper frequency is set between 1kHz and 2KHz.

Under chopper mode, the input noise peak-to-peak voltage in FS9932 is less than 0.5μV (0.1Hz~1Hz). But an equivalent input current of less than 100pA is generated, due to the effect of switching.

11.11.1 Single End Amplifier Application

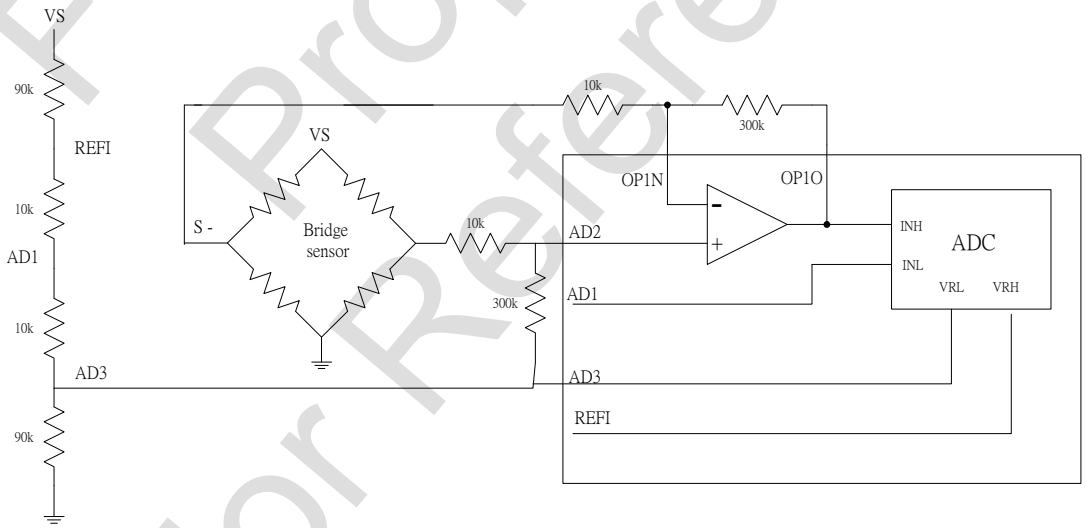
Measurement of small signal usually takes consideration of the drifting of an OPAMP offset voltage. In the Figure below, the negative input is connected to AGND. It is also possible to measure the ADC's negative input and deduct this value in order to correct the error caused by the Amplifier's offset voltage drifting. Because AGND provides current output in applications, AD2 is used as negative input measurement point to avoid unnecessary voltage error.

OPAMP input offset is amplified by an amplifier then inputted to ADC. Too much amplification can cause OPAMP output move beyond ADC linear operation range. Hence, under normal conditions, OPAMP amplification should be less than 50 times.



11.11.2 Differential Amplifier

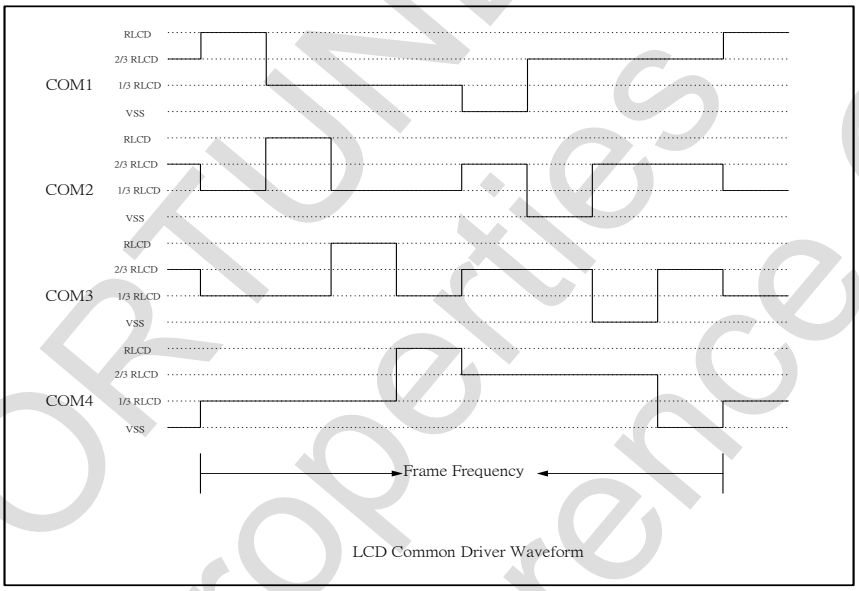
Measurement of differential signal is often used in bridge sensor applications. As shown in the differential amplifier below, VS Pin is used as power input for bridge sensor, ADC reference voltage is also from VS Pin after voltage division. When there is a small change in VS, ADC output does not change. Connecting AD1 to ADC negative input can adjust the zero point of bridge sensor. When starting chopper mode, the amplification should be less than 100 times.



11.12 LCD Driver and Output Port

Address	Name	Content							
40H	LCD1	SEG1 [3:0]				SEG0 [3:0]			
42H	PT5O							PT5 [1:0]	
43H	PT6O							PT6 [1:0]	
4CH	LCD6	SEG11 [3:0]				SEG10 [3:0]			
50H	LCD5	SEG9 [3:0]				SEG8 [3:0]			
51H	LCD4	SEG7 [3:0]				SEG6 [3:0]			
52H	LCD3	SEG5 [3:0]				SEG4 [3:0]			
53H	LCD2	SEG3 [3:0]				SEG2 [3:0]			
54H	LCDENR	LCDCKS [1:0]		LCDEN		S_LCDO [1:0]			

- LCD Common Driver Waveform



LCD Common Driver Waveform

- LCDEN =1 starts the LCD clock. LCD1~LCD6 is the LCD display data area.
- LCDCKS [1:0] select LCD frame frequency.

LCDCKS [1:0]	LCD frame frequency
00	LCD Input Frequency/8
01	LCD Input Frequency/16
10	LCD Input Frequency/32
11	LCD Input Frequency/64

- S_LCDO [1:0] select LCD segment output as general output port.

	General Output Port
S_LCDO [0]=1	SEG8~SEG9
S_LCDO [1]=1	SEG10~SEG11

11.13 CPU Reset

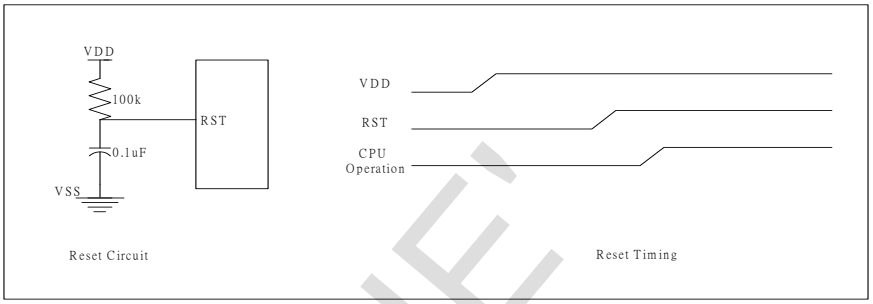
FS9932 CPU has three reset signals and they are external RST pin, low voltage reset(LVR), and watchdog time out reset. When resetting, CPU's Program Counter (PC) is reset to 0. After reset, CPU starts working. The following table shows the CPU's internal register status after reset.

Address	Name	External Reset & LVR	WDT Reset
02H	FSR0	uuuuuuuu	uuuuuuuu
03H	FSR1	uuuuuuuu	uuuuuuuu
04H	STATUS	00000uuu	uuuu1uuu
05H	WORK	uuuuuuuu	uuuuuuuu
06H	INTF	u0000000	u0000000
07H	INTE	u0000000	u0000000
08H	MCK	00000000	00000000
09H	PCK	uuuu0000	uuuu0000
0CH	TMOUT	00000000	00000000
0DH	TMCON	u0000000	u0000000
10H	ADOH	00000000	00000000
11H	ADOL	00000000	00000000
13H	ADCON	uuuu0000	uuuu0000
20H	PT1	uuuuuuuu	uuuuuuuu
21H	PT1EN	00000000	uuuuuuuu
22H	PT1PU	00000000	uuuuuuuu
23H	PT1MR	00000000	uuuuuuuu
24H	PT2	uuuuuuuu	uuuuuuuu
25H	PT2EN	00uuuuuu	uuuuuuuu
26H	PT2PU	00uuuuuu	uuuuuuuu
27H	PT2MR	00uuuuuu	uuuuuuuu
29H	NETA	00000000	00000000
2AH	NETB	00000000	00000000
2CH	NETD	00000000	00000000
2EH	NETF	00000000	00000000
2FH	NETG	00000000	00000000
30H	NETH	00000000	00000000
32H	NETJ	00000000	00000000
33H	NETK	00000000	00000000
34H	PWDH	00000000	00000000
35H	PWDL	00000000	00000000
36H	PWCON	00000000	00000000
40H	LCD1	uuuuuuuu	uuuuuuuu
42H	PT5O	uuuuuuuu	uuuuuuuu
43H	PT6O	uuuuuuuu	uuuuuuuu
4CH	LCD6	uuuuuuuu	uuuuuuuu
50H	LCD5	uuuuuuuu	uuuuuuuu
51H	LCD4	uuuuuuuu	uuuuuuuu
52H	LCD3	uuuuuuuu	uuuuuuuu
53H	LCD2	uuuuuuuu	uuuuuuuu
54H	LCDENR	00000000	00000000

■ Note: "u" means unknown or unchanged.

11.13.1 External RST Pin

When RST Pin is Low, CPU is in Reset status. The external R/C circuit is shown as follows. When VDD changes from “low” to “high”, a Reset signal will be generated to bring CPU back to normal operation condition.

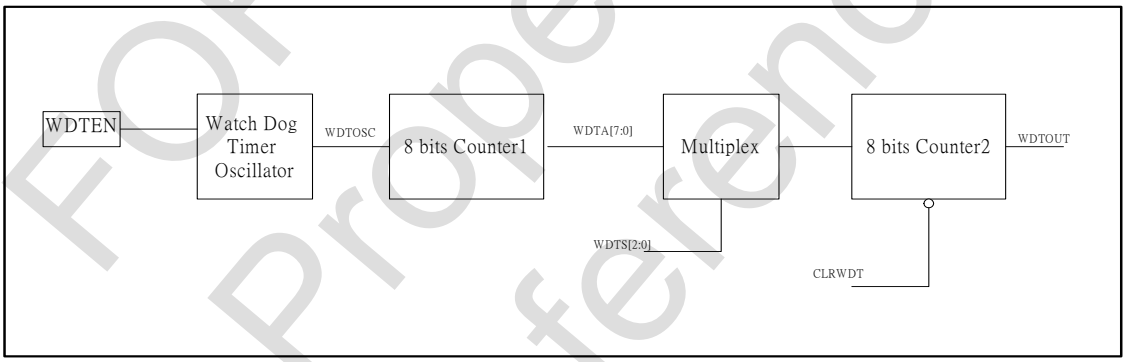


11.13.2 Low Voltage Reset

To avoid putting CPU in an abnormal power status that makes CPU unable to reset and causes CPU operating abnormally, FS9932 contains a low voltage reset circuit. When VDD of FS9932 VDD is less than LVR, CPU enters reset status.

11.13.3 Watchdog Time Out Reset

Address	Name	Content							
04H	STATUS					TO			
0DH	TMCON		WTS [2:0]						



When starting watch dog timer, it is necessary to connect WDTEN pin to VDD. Otherwise, connect it to VSS. When using CLRWDT instruction, WDT Counter may be reset. The clock input of Watch dog timer comes from an independent R/C oscillator. The Watch dog time output can be selected by WTS, as shown in the following table. When watch dog time output happens, CPU enters reset status and set TO bit to 1.

Typical Frequency of WDTOSC is about 1.376kHz.		
WTS[2:0]	**Frequency of WDTOUT**	**Typical Frequency of WDTOUT**
000	FWDTOSC / 65536	23.7mHz
001	FWDTOSC / 32768	42.02mHz
010	FWDTOSC / 16384	84.03mHz
011	FWDTOSC / 8192	166.7mHz
100	FWDTOSC / 4096	359.7mHz
101	FWDTOSC / 2048	675.7mHz
110	FWDTOSC / 1024	1.347Hz
111	FWDTOSC / 512	2.688Hz

11.14 Halt and Sleep Mode

11.14.1 Halt Mode

After CPU executes a HALT command, CPU program counter (PC) stops counting until an interrupt command is issued. To avoid program errors caused by Interrupt return, it is suggested to add a NOP command after HALT to guarantee the program's normal execution.

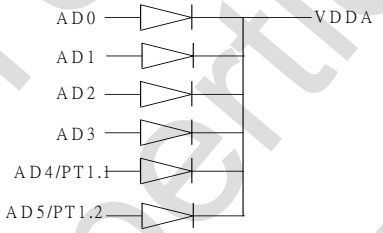
```
HALT
NOP
```

11.14.2 Sleep Mode

After CPU executes SLEEP command, all oscillators stop working until an external interrupt command is issued or the CPU is reset. To avoid program errors caused by Interrupt return, it is suggested to add a NOP command after SLEEP to guarantee the program's normal execution.

```
SLEEP
NOP
```

To make sure that CPU consumes minimum power in SLEEP mode, it is necessary to open all power blocks and analog circuits before issuing the SLEEP command, and make sure all I/O ports are in VDD or VSS voltage levels. There exist parasitic diodes between VDDA and analog input ports (see below figure). When VDDA is turned off and VDDA is low, it is necessary to keep AD0~AD3 in floating or low voltage, and AD4/PT1.1, AD5/PT1.2 output low.

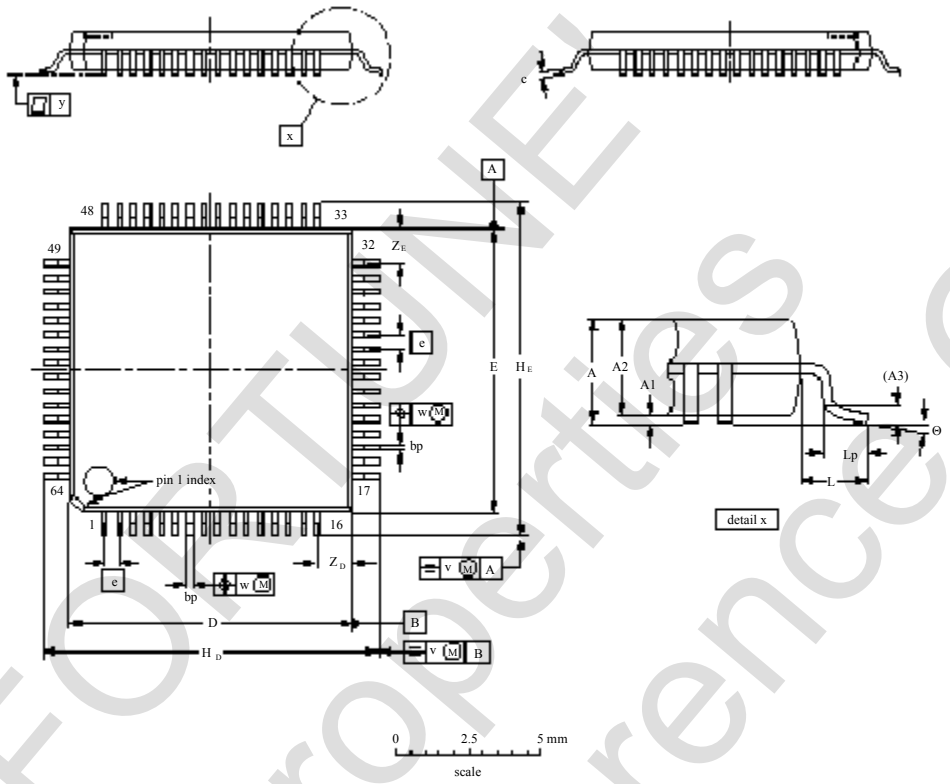


It is recommended that users execute the following program before issuing the SLEEP command.

```
CLRF NETA
CLRF NETB
CLRF NETD
CLRF NETF
CLRF NETG
CLRF NETH
CLRF NETJ
CLRF PT2PU
MOVLW   0FFh
MOVWF   PT2EN
CLRF PT2                ; Set PT2 Output Low
MOVLW   01h
MOVWF   PT1PU
MOVLW   0FEh
MOVWF   PT1EN
CLRF PT1                ; Set PT1 [7:1] Output Low, PT1 [0] Input /Pull up
CLRF INTF
MOVLW   081h            ; External Interrupt Enable
MOVWF   INTE
SLEEP
NOP
```

12. Package Outline

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x1.4 mm

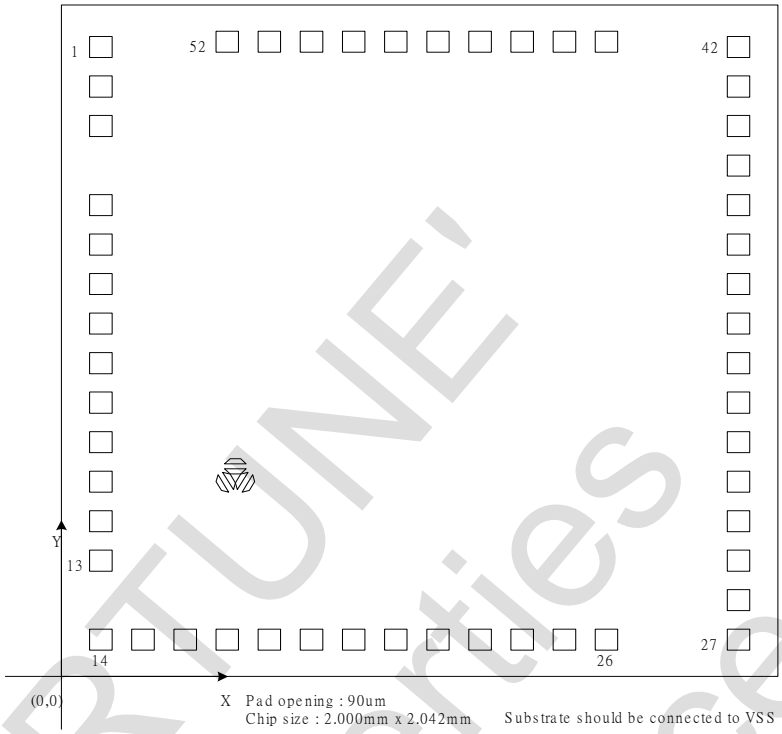


DIMENSIONS (mm are the originl dimensions)

UNIT	A max.	A1	A2	A3	bp	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	Lp	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	Θ
mm	1.60	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.2	0.12	0.075	1.45 1.05	1.45 1.05	7 ° 0 °

Note: 1.Plastic or metal protrusions of 0.25 mm maximum per side are not included.

13. PAD Assignment



14. Pad Coordinate

Pad No.	Name	X [mm]	Y [mm]	Pad No.	Name	X [mm]	Y [mm]
1	TST	0.072	1.910	27	SEG11	1.927	0.078
2	RST	0.072	1.790	28	SEG10	1.927	0.198
3	WDTEN	0.072	1.670	29	SEG9	1.927	0.318
4	PT2<7>	0.072	1.458	30	SEG8	1.927	0.438
5	PT2<6>	0.072	1.338	31	SEG7	1.927	0.558
6	PT1<7>	0.072	1.218	32	SEG6	1.927	0.678
7	PT1<6>	0.072	1.098	33	SEG5	1.927	0.798
8	PT1<5>	0.072	0.978	34	SEG4	1.927	0.918
9	PT1<4>	0.072	0.858	35	SEG3	1.927	1.038
10	PT1<3>	0.072	0.738	36	SEG2	1.927	1.158
11	PT1<2>	0.072	0.618	37	SEG1	1.927	1.278
12	PT1<1>	0.072	0.497	38	SEG0	1.927	1.398
13	PT1<0>	0.072	0.377	39	COM4	1.927	1.518
14	VSS	0.117	0.075	40	COM3	1.927	1.638
15	OP1N	0.241	0.075	41	COM2	1.927	1.758
16	OP1O	0.361	0.075	42	COM1	1.927	1.878
17	REFO	0.481	0.075	43	VS	1.575	1.970
18	REFI	0.601	0.075	44	VDDA	1.456	1.970
19	FT1	0.721	0.075	45	VGG	1.336	1.970
20	FT2	0.841	0.075	46	VSSP	1.216	1.970
21	AD0	0.961	0.075	47	CB	1.096	1.970
22	AD1	1.081	0.075	48	CA	0.976	1.970
23	AD2	1.201	0.075	49	VDDP	0.856	1.970
24	AD3	1.321	0.075	50	VDD	0.736	1.970
25	VB	1.441	0.075	51	XOUT	0.616	1.970
26	AGND	1.561	0.075	52	XIN	0.491	1.970

15. Revision History

Ver.	Date	Page	Description
1.3	2004/04/05	-	Reformat and correct the contents
1.4	2005/11/07	5	Add FS9934 information in Ordering Information.
		10	Add FS9934 resolution and ADC linearity error in ADC Characteristics.
		44	Add Revision History.
1.5	2005/11/28	5	Add FS9934B information in Ordering Information.
		11	Add FS9934B resolution and ADC linearity error in ADC Characteristics.
1.6	2014/05/22	2	Revised company address